IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2364
Chu	Art Unit: 2666
Application No.: 09/668,407	Examiner: Michael J. Moore Jr.
Filed: September 22, 2000	Atty. Docket: 2222.4180001
For: **Multiple-Buffer Queueing Of Data Packets With High Throughput Rate**	

Brief on Appeal Under 37 C.F.R. § 41.37

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal from the final rejection of claims 1-11, 17-27, and 33-43 was filed on February 9, 2006. Appellant hereby files one copy of this Appeal Brief, together with the required fee set forth in 37 C.F.R. § 41.20(b)(2).

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

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I. Real Party In Interest (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is the United States of America as represented by the Secretary of the Navy, having its principal place of business at the Naval Research Laboratory, 4555 Overlook Avenue, S.W., Washington, D.C. 20375-5320. In addition, Nanocomm Systems, LLC, located at 2215 B Renaissance Drive, Suite 5, Las Vegas, NV 89119 is a licensee under this application.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

To the best of the knowledge of Appellant, Appellant's legal representative, and Appellant's assignee, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on a decision by the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.

III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))

This application was originally filed as U.S. Application No. 09/668,407 on September 22, 2000 with 48 claims. In response to an Office Action mailed May 19, 2004, Appellant filed an Amendment and Reply on September 29, 2004 in which claims 1-3, 12, 13, 17-19, 28, 29, 34, 35, 44, and 45 were amended. In response to a second Office Action mailed January 24, 2005, Appellant filed a second Amendment and Reply on May 13, 2005, in which claims 1, 17, and 33 were amended. The Examiner issued a Final Office Action on August 9, 2005.

Claims 1-48 are pending. Claims 1-11, 17-27, and 33-43 are rejected; claims 12-16, 28-32, and 44-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, claims 1-11, 17-27, and 33-43 are being appealed. A copy of the claims on appeal can be found in the attached Appendix as required under 37 C.F.R. § 41.37(c)(1)(viii).

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

All amendments presented in the Amendment and Reply dated September 29, 2004 and the Amendment and Reply dated May 13, 2005 have been entered.

V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

The present invention is directed to data buffering in computer networks. (Specification, p. 1, lines 6-7). As a particular kind of network, Appellant's specification refers to a synchronous optical network (SONET). (Specification, p. 1, lines 11-14). SONET is a standard for communicating digital information across a group of elements in a fiber-optics network using lasers and light emitting diodes (LEDs).

FIG. 2 of the Specification, reprinted below, illustrates an exemplary high-level block diagram of a data buffer circuit, in accordance with the subject matter claimed. Independent claim 1 is directed to an apparatus including a buffer memory 220 and a packet memory 230. (Specification, FIG. 2, reproduced below).

Buffer memory 220 stores data belonging to a network connection in the form of a linked list. (Specification, p. 6, lines 16-17). A buffer management controller (BMC) 210 receives data in an ingress queue 510 that buffers the data stream. (Specification, p. 10, lines 3-4). BMC 210 passes the data on a data bus 225 to buffer memory 220. (Specification, p. 6, lines 16-17). Buffer memory 220 comprises a plurality of input queues 410, each corresponding to a connection identifier, as shown in FIG. 4. (Specification, p. 9, lines 10-18; FIG. 4). BMC 210 determines the connection identifier associated with a connection and transfers the data to a corresponding input buffer in buffer memory 220. (Specification, p. 11, lines 21-24).

Packet memory 230 receives data transferred from buffer memory via a data bus 235 and transmits data to output buffer memory 240. (Specification, p. 6, lines 21-23). The data that is transferred to packet memory 230 is collapsed into chunks of data to speed up data transfer from input buffer memory 220 to output buffer memory 240. (Specification, p. 8, lines 5-6).

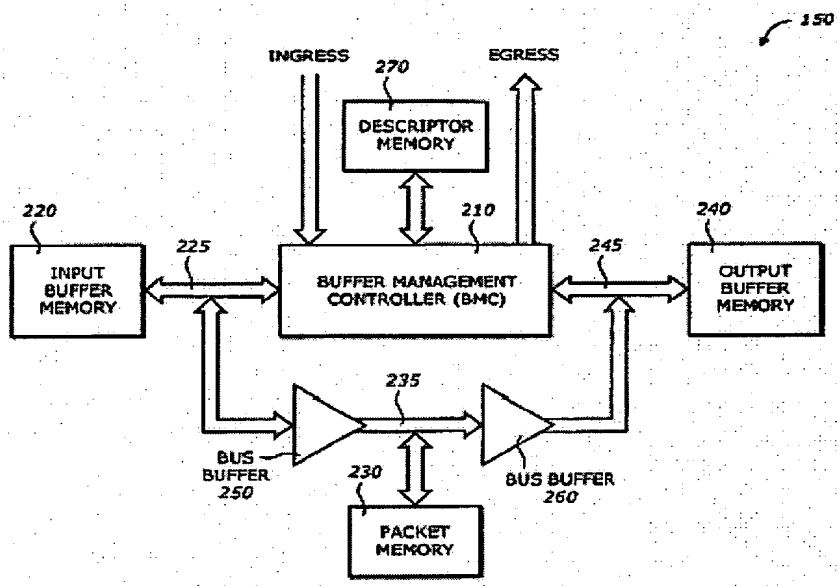

FIG. 2

Buffer memory 220 is of a different type than packet memory 230. (Specification, p. 6, lines 18-19). For example, buffer memory 220 may be implemented as static random access memory (SRAM), and packet memory 230 may be implemented as synchronous dynamic random access memory (SDRAM). (Specification, p. 6, lines 19-21; lines 23-25).

The block diagram of the buffer circuit shown in FIG. 2 also includes a descriptor memory 270. (Specification, FIG. 2). Descriptor memory 270 stores descriptor information relating to the chunks of data that are stored in input buffer memory 220, packet memory 230, and output buffer memory 240. (Specification, p. 6, line 32 - p. 7, line 1). For example, the descriptor information may include pointers to portions of the data stream. (Specification, p. 7, lines 1-2).

Independent claims 17 and 33, and their respective dependent claims, find similar support to the above in the specification.

VI. Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. § 41.37(c)(1)(vi))

The Examiner finally rejected claims 1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43 under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,401,147 to Sang *et al.* ("Sang *et al.*").

The Examiner finally rejected claims 3-7, 19-23, and 35-39 under 35 U.S.C. § 103(a) as allegedly being obvious over Sang *et al.* in view of the U.S. Patent No. 6,542,502 to Herring *et al.* ("Herring *et al.*").

Accordingly, the grounds of rejection to be reviewed on appeal are:

A. Ground 1

Whether claims 1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43 are anticipated by Sang *et al.* under 35 U.S.C. § 102(e).

B. Ground 2

Whether claims 3-7, 19-23, and 35-39 would have been obvious over Sang *et al.* in view of Herring *et al.* under 35 U.S.C. § 103(a).

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

There are two separate grounds of rejection to be reviewed on appeal.

A. Rejection of Claims 1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43 under 35 U.S.C. § 102(e) as Anticipated by Sang et al.

A Final Office Action was mailed on August 9, 2005, rejecting claims 1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43 under 35 U.S.C. § 102(e) as anticipated by Sang *et al.*

To establish a *prima facie* case of anticipation, the Examiner must show that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Because the Examiner has failed to establish that each and every element is described in Sang *et al.*, the rejection of claims 1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43 is in error and must be reversed.

1. The Anticipation Rejection with Respect to Claims 1, 17, and 33 is in Error and Must be Reversed

Independent claims 1, 17, and 33 each require a connection identifier that identifies a connection in a channel in a network. Specifically, claims 1 and 17 recite, among other features, "a connection identifier corresponding to a channel in a network, . . . , the connection identifier identifying a connection in the channel"; and claim 33 recites, among other features, "a channel in a network . . . the connection identifier identifying a connection in the channel." Appellant's remarks focus on independent claim 1 because these remarks apply equally to independent claims 17 and 33 by virtue of the above-referenced language recited in each independent claim.

Sang *et al.* does not teach or suggest each and every element of independent claim 1. Specifically, Sang *et al.* does not teach or suggest a connection identifier

corresponding to a channel in a network that identifies a connection in the channel, as recited in independent claim 1.

In the Final Rejection, the Examiner states:

> Regarding claim 1, "a buffer memory of a first type to store data associated with a connection identifier corresponding to a channel in a network" is anticipated by input queue write side 410 (buffer memory of first type) of Figure 4 that receives and stores frame pointer entries (data) that point (associate) to buffers (connection identifier) in external memory as spoken of on column 10, line 66 — column 11, line 3.

(Final Office Action dated August 9, 2005, at p. 2).

The Examiner goes on to state:

> "The connection identifier identifying a connection in the channel" is anticipated by the buffers (connection identifier) in external memory that store (indicate) specific bytes of data frames as spoken of on column 11, lines 1-3.

(*Id.*).

The Examiner appears to be equating the buffers of Sang *et al.* with the connection identifier recited in independent claim 1. However, none of the elements disclosed in Sang *et al.*, including the buffers listed by the Examiner, correspond to a connection identifier. The Examiner appears to misapprehend the term "connection identifier," as recited in independent claim 1.

A connection identifier identifies a network connection, i.e., a connection between at least two elements in a group of elements that are linked together to share resources. For example, Appellant's specification refers to an exemplary network—namely, SONET. (*See* Specification, p. 1, lines 11-14; p. 5, line 1 - p. 6, line 2). In terms of SONET (or any similar type of network), a connection identifier would have been understood by a person skilled in the art to mean header information corresponding to a particular connection between two destinations in the network. With this background,

Appellant's specification describes how data stored in a buffer memory is associated with a connection identifier that corresponds to a channel in a network:

> The input buffer memory 220 includes K input buffer queues 410_1 to 410_K and corresponding K threshold detectors 420_1 to 420_K. Each of the K input buffer queues 410_1 to 410_K is associated with a connection identifier. There are K connection identifiers correspond[ing] to K input buffer queues 410_1 to 410_K.

(Specification, p. 9, lines 11-15). Appellant's specification goes on to describe how the connection identifier is used to organize the data into an appropriate queue:

> The buffer management controller 210 determines the connection identifier associated with the connection and transfers the data to the corresponding input buffer queue in the input buffer memory 220.

(*Id.*, p. 11, lines 21-24).

In Sang *et al.*, the method of buffering data packets is described in terms of a multiport switch **12**. (Sang *et al.*, FIG. 2). A multiport switch enables communication of data packets between elements in a network by selectively forwarding data packets to appropriate destinations based upon network protocols. (*Id.*, col. 4, lines 55-68). The multiport switch **12** includes an external memory interface **44** that enables external storage of packet data in an external memory **36**. (*Id.*, col. 6, lines 10-11). The multiport switch **12** achieves minimized chip size, while maintaining sufficient storage capacity, by using the external memory to store received data frames and memory structures. (*Id.*, col. 6, lines 10-16).

The buffers in external memory **36** that store specific bytes of data frames are not connection identifiers. As described above, a connection identifier includes header information that uniquely identifies a connection between elements in a network. The link between the multiport switch **12** and the external memory **36** is not a network connection. In fact, the external memory **36** is not even a separate element in the network. The multiport switch **12** merely "uses the external memory **36** for storage of

received frame data and memory structures." (*Id.*, col. 6, lines 14-16). Thus, a buffer in the external memory **36** cannot possibly be interpreted as a connection identifier that identifies a network connection between the external memory **36** and the multiport switch **12**, because the external memory **36** and the multiport switch **12** are not even separate elements in the network.

Accordingly, Sang *et al.* does not teach or suggest each and every feature of independent claim 1, because Sang *et al.* fails to teach a connection identifier. Therefore, independent claim 1 is patentable over Sang *et al.* Furthermore, for at least the same reasons as described with respect to claim 1, and further in view of their own respective features, independent claims 17 and 33 are also patentable over Sang *et al.* Consequently, the Examiner's rejection of claims 1, 17, and 33 is in error and must be reversed.

2. The Anticipation Rejection with Respect to Claims 2, 18, and 34 is in Error and Must be Reversed

Claims 2, 18, and 34 are each patentable over Sang *et al.* for at least the same reasons as described above with respect to claims 1, 17, and 33, from which claims 2, 18, and 34 respectively depend. Furthermore, claims 2, 18, and 34 are also patentable over Sang *et al.* for the reasons set forth below.

Claims 2, 18, and 34 each recite descriptor information stored in a descriptor memory. Specifically, claims 2 and 34 recite, among other features, "a descriptor memory to store descriptor information corresponding to the at least one chunk"; and claim 18 recites, among other features, "storing descriptor information corresponding to the at least one chunk in a descriptor memory." Appellant's remarks focus on claim 2 because these remarks apply equally to claims 18 and 34 by virtue of the above-referenced language recited in each claim.

Sang *et al.* does not teach or suggest each and every element of claim 2. Specifically, Sang *et al.* does not teach or suggest a descriptor memory that stores descriptor information corresponding to at least one chunk, as recited in claim 2.

In the Final Rejection, the Examiner states:

> Regarding claim 2, "a descriptor memory to store descriptor information corresponding to the at least one chunk" is anticipated by queue overflow storage area 414 (descriptor memory) of Figure 4.

(Final Office Action dated August 9, 2005, at p. 3).

The Examiner equates the queue overflow storage area 414 of Sang *et al.* with the descriptor memory recited in claim 2. However, none of the elements of the multiport switch disclosed in Sang *et al.*, including the queue overflow storage area 414 listed by the Examiner, correspond to a descriptor memory. The Examiner appears to misapprehend the term "descriptor memory," as recited in claim 2.

Appellant's specification describes the descriptor memory with reference to FIG. 2:

> The descriptor memory 270 stores descriptor information regarding the chunks stored in the input buffer memory 220, the packet memory 230, and the output buffer memory 240. Examples of the descriptor information include pointers to the head and tail chunks, described later, of the data stream.

(Specification, p. 6, line 32 - p. 7, line 2; FIG. 2). Appellant's specification goes on to describe the head and tail chunks with reference to FIG. 3A:

> The head chunk 310, the linking chunks 320_1 to 320_N, and the tail chunk 330 store data at the beginning, in the middle, and at the end of a data stream. Each of the chunks stores a fixed-size block of data. The tail chunk 330 may contain no data or partially filled block of data depending on the size of the data stream and the size of each chunk. Each of the chunks has a chunk header and a chunk data block. The chunk header contains information about the corresponding chunk and the chunk data block contains the data in the data stream. The head chunk 310 has a chunk header 312 and a chunk data block 314. The linking chunks have chunk headers 322_1 to 322_N and chunk data blocks 324_1 to 324_N. The tail chunk 330 has a chunk header 332 and a chunk data block 334.

(*Id.*, p. 7, lines 7-16; FIG. 3A).

Thus, the descriptor memory 270 stores descriptor information, such as pointers and headers, relating to data blocks; the descriptor memory 270 does not store the data blocks themselves.

In stark contrast, the queue overflow storage area of Sang *et al.* stores *data*, not *descriptor information* (e.g., pointers to the data). In Sang *et al.*, if there is too much data arriving at the read side of the multiport switch, the data is stored in the queue overflow storage area. (Sang *et al.*, col. 11, lines 55-59). In other words, the queue overflow storage area of Sang *et al.* is used to avoid an overflow of data, not to store information relating to the data. Thus, the queue overflow storage area cannot possibly correspond to the descriptor memory recited in claim 2.

Accordingly, the Examiner has failed to establish that Sang *et al.* teach the descriptor memory recited in claim 2. Similarly, the Examiner has failed to establish that Sang *et al.* teach the descriptor memory recited in claims 18 and 34. For at least the foregoing reasons, claims 2, 18, and 34 are patentable over Sang *et al.* and the rejection of these claims must be reversed.

3. The Anticipation Rejection with Respect to Claims 8-11, 24-27, and 40-43 is in Error and Must be Reversed

Claims 8-11, 24-27, and 40-43 are each patentable over Sang *et al.* for at least the same reasons as described above with respect to claim 2 (from which claims 8-11 depend), claim 18 (from which claims 24-27 depend), and claim 34 (from which claims 40-43 depend). Furthermore, claims 8-11, 24-27, and 40-43 are also patentable over Sang *et al.* for the reasons set forth below. Appellant's remarks focus mainly on claims 8, 24, and 40, because any claim which depends from a patentable claim is also patentable by virtue of its dependency.

Claims 8 and 40 each recite, among other features, "an ingress queue to buffer the data stream of a packet from an ingress of the channel, the packet having a packet size; and a queue segmenter to chunk the data stream into the at least one chunk." Claim 24 recites a method for practicing the apparatus and system recited in claims 8 and 40, respectively. Accordingly, claim 8 is representative of these claims.

Sang *et al.* does not teach or suggest each and every element of claim 8. Specifically, Sang *et al.* does not teach or suggest an ingress queue as recited in claim 8.

In the Final Rejection, the Examiner states:

> "[A]n ingress queue to buffer the data stream of a packet from an ingress of the channel, the packet having a packet size" and "a queue segmenter to chunk the data stream into the at least one chunk" is anticipated by queue overflow engine 416 of Figure 4 that determines whether to directly pass the pending entry from queue write side 410 (ingress) to the queue read side 412 or to burst write the data to the overflow storage area 414 as spoken of on column 11, lines 8-26.

(Final Office Action dated August 9, 2005, at pp. 3-4).

However, none of the elements disclosed in Sang *et al.*, including the queue overflow engine 416 listed by the Examiner, correspond to the ingress queue. The Examiner appears to misapprehend the term "ingress queue," as recited in claim 8.

Appellant's specification describes the ingress queue, and its relationship to the queue segmenter as follows:

> The ingress queue 510 buffers the data stream coming from the ingress of the channel on the input data path. The ingress queue 510 acts as a temporary storage for the data stream before being loaded into the input buffer memory 220. The queue segmenter 515 slices the data from the ingress queue 510 into blocks of data of fixed size so that they can be transferred to the input buffer queues of the input buffer memory 220.

(Specification, p. 10, lines 3-8; FIG. 5).

Thus, the ingress queue buffers the data stream, and the queue segmenter segments the buffered data stream into blocks of data of fixed size.

The queue overflow engine 416 of Sang *et al.* does not correspond to the ingress queue recited in claim 8. Unlike the ingress queue, the queue overflow engine of Sang *et al.* is described as decision-making logic, not a buffer. (Sang *et al.*, col. 11, lines 8-10). In Sang *et al.*, the queue overflow engine 416 passes entries from the read side directly to the write side under one set of conditions, and burst writes the entries into external memory under a different set of conditions. (*Id.*, col. 11, lines 10-15; lines 20-23). The queue overflow engine 416 of Sang *et al.* does not buffer the data stream like the ingress queue recited in claim 8.

Accordingly, the Examiner has failed to establish that Sang *et al.* teach the ingress queue recited in claim 8. Similarly, the Examiner has failed to establish that Sang *et al.* teach the ingress queue recited in claims 24 and 40. For at least these further reasons, claims 8, 24, and 40 are patentable over Sang *et al.* and the rejection of these claims must be reversed.

For at least the foregoing reasons, claims 9-11, 25-27, and 41-43 are also patentable over Sang *et al.* and the rejection of these claims must be reversed.

B. Rejection of claims 3-7, 19-23, and 35-39 under 35 U.S.C. § 103(a) as being obvious over Sang et al. in view of Herring et al.

The Final Office Action, mailed on August 9, 2005, rejected claims 3-7, 19-23, and 35-39 under 35 U.S.C. § 103(a) as being obvious over Sang *et al.* in view of Herring *et al.*

The Obviousness Rejection with Respect to Claims 3-7, 19-23, and 35-39 is in Error and Must be Reversed

In proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a *prima facie* case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1471-73 (Fed. Cir. 1984). To establish a *prima facie* case of obviousness under 35

U.S.C. § 103, every claim limitation must be taught, or obvious to a person of ordinary skill in the art, in the combination of the references. *See Orthopedic Equipment, Inc. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983). In addition, some motivation or suggestion must exist in the reference or in the knowledge generally available to one of ordinary skill in the art to combine the references. *Id.* Finally, the reference must reveal a reasonable expectation of success. *Id.* Because the Examiner has failed to establish all of these criteria, the rejection of claims 3-7, 19-23, and 35-39 must be reversed.

Sang *et al.* and Herring *et al.*, alone or in combination, fail to teach or suggest each and every feature of claim 3. Claim 3 depends from claim 2, which in turn depends from claim 1. As set forth above, Sang *et al.* fails to teach or suggest each and every feature of claims 1 and 2. Herring *et al.* does not overcome the deficiencies of Sang *et al.* with respect to claim 1, let alone the deficiencies of Sang *et al.* with respect to claim 2. Specifically, Herring *et al.* do not teach or suggest the connection identifier nor the descriptor memory missing from Sang *et al.* For at least these reasons and further in view of its features, claim 3 is patentable over the combination of Sang *et al.* and Herring *et al.* Therefore, the rejection of claim 3 is in error and must be reversed. Furthermore, dependent claims 4-7 are also not rendered obvious by the combination of Sang *et al.* and Herring *et al.* for at least the same reasons as claim 3 from which they depend, and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 4-7 are also in error and must be reversed.

Claim 19 recites a method for practicing the invention recited in claim 3, and claim 35 recites a system for practicing the invention recited in claim 3. Thus, claims 19 and 35 are also patentable over the combination of Sang *et al.* and Herring *et al.* for at least the same reasons as set forth above with respect to claim 3. Therefore, the rejection of claims 19 and 35 is in error and must be reversed. Furthermore, claims 20-23 and 36-

39 are also not rendered obvious by the combination of Sang *et al.* and Herring *et al.* for at least the same reasons as claim 19 (from which claims 20-23 depend) and claim 35 (from which claims 36-39 depend). Accordingly, the Examiner's rejection of claims 20-23 and 36-39 is also in error and must be reversed.

C. Conclusion

Claims 1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43 are patentable over Sang *et al.* because the Examiner has failed to establish that Sang *et al.* anticipate these claims. Claims 3-7, 19-23, and 35-39 are patentable over Sang *et al.* in view of Herring *et al.* because the Examiner has failed to make a *prima facie* case of obviousness. Thus, the subject matter of claims 1-11, 17-27, and 33-43 is patentable over the cited art. Therefore, Appellants respectfully request that the Board reverse the Examiner's final rejection of these claims and remand this application for issue.

Respectfully submitted,

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VIII. Claims Appendix

1. An apparatus comprising:

a buffer memory of a first type to store data associated with a connection identifier corresponding to a channel in a network, the data being organized into at least one chunk based on a linked list, the connection identifier identifying a connection in the channel, the data being part of a data stream associated with the connection; and

a packet memory of a second type coupled to the buffer memory to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory.

2. The apparatus of claim 1 further comprises:

a descriptor memory to store descriptor information corresponding to the at least one chunk; and

a controller coupled to the descriptor memory and the buffer memory to control data transfer between the buffer memory and the packet memory using the descriptor information.

3. The apparatus of claim 2 wherein the at least one chunk comprises:

a chunk header to store chunk information associated with the linked list; and

a chunk data block to store the data.

4. The apparatus of claim 3 wherein the chunk information includes at least one of a pointer to point to one other chunk, a size specifier to specify size of the at least one chunk, and a type specifier to specify type of the at least one chunk.

5. The apparatus of claim 4 wherein the at least one chunk is one of a head chunk corresponding to one end of the data stream, a linking chunk corresponding to an intermediate portion of the data stream, and a tail chunk corresponding to one other end of the data stream.

6. The apparatus of claim 5 wherein the descriptor information includes at least one of head and tail pointers, the head and tail pointers pointing to the head and tail chunks, respectively.

7. The apparatus of claim 6 wherein the connection identifier points to one of the head and tail pointers.

8. The apparatus of claim 2 wherein the controller comprises:

an ingress queue to buffer the data stream of a packet from an ingress of the channel, the packet having a packet size; and

a queue segmenter to chunk the data stream into the at least one chunk.

9. The apparatus of claim 8 wherein the buffer memory comprises an input buffer memory to store the at least one chunk transferred from the queue segmenter.

10. The apparatus of claim 9 wherein the input buffer memory comprises a queue associated with the connection identifier, the queue having a threshold and being configured to store the at least one chunk.

11. The apparatus of claim 10 wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request.

17. A method comprising:

storing data associated with a connection identifier corresponding to a channel in a network in a buffer memory of a first type, the data being organized into at least one chunk based on a linked list, the connection identifier identifying a connection in the channel, the data being part of a data stream associated with the connection; and

providing access to the stored data using a packet memory of a second type when a transfer condition occurs, such that the data is transferred between the buffer memory and the packet memory.

18. The method of claim 17 further comprises:

storing descriptor information corresponding to the at least one chunk in a descriptor memory; and

controlling data transfer between the buffer memory and the packet memory using the descriptor information.

19. The method of claim 18 wherein storing the data comprises:

storing chunk information associated with the linked list in a chunk header; and

storing the data in a chunk data block.

20. The method of claim 19 wherein the chunk information includes at least one of a pointer to point to one other chunk, a size specifier to specify size of the at least one chunk, and a type specifier to specify type of the at least one chunk.

21. The method of claim 20 wherein the at least one chunk is one of a head chunk corresponding to one end of the data stream, a linking chunk corresponding to an intermediate portion of the data stream, and a tail chunk corresponding to one other end of the data stream.

22. The method of claim 21 wherein the descriptor information includes at least one of head and tail pointers, the head and tail pointers pointing to the head and tail chunks, respectively.

23. The method of claim 22 wherein the connection identifier points to one of the head and tail pointers.

24. The method of claim 18 wherein controlling the data transfer comprises:

buffering the data stream of a packet from an ingress of the channel by an ingress queue, the packet having a packet size; and

segmenting the data stream into the at least one chunk.

25. The method of claim 24 wherein storing the data comprises storing the at least one chunk transferred from the queue segmenter in an input buffer memory.

26. The method of claim 25 wherein storing the at least one chunk in the input buffer memory comprises storing the at least one chunk in a queue associated with the connection identifier, the queue having a threshold.

27. The method of claim 26 wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request.

33. A system comprising:

a channel in a network having an ingress and egress;

a data buffer circuit coupled to the channel to buffer data transmitted over the channel, the data buffer circuit comprising:

an input buffer memory of a first type to store data associated with a connection identifier corresponding to the channel, the data being organized into at least one chunk based on a linked list, the connection identifier identifying a connection in the channel, the data being part of a data stream associated with the connection,

an output buffer memory of the first type to store the data transferred from the input buffer memory, and

a packet memory of a second type coupled to the input and output buffer memories to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory.

34. The system of claim 33 wherein the data buffer circuit further comprises:

a descriptor memory to store descriptor information corresponding to the at least one chunk; and

a controller coupled to the descriptor memory and the input and output buffer memories to control data transfer between the buffer memories and the packet memory using the descriptor information.

35. The system of claim 34 wherein the at least one chunk comprises:

a chunk header to store chunk information associated with the linked list; and

a chunk data block to store the data.

36. The system of claim 35 wherein the chunk information includes at least one of a pointer to point to one other chunk, a size specifier to specify size of the at least one chunk, and a type specifier to specify type of the at least one chunk.

37. The system of claim 36 wherein the at least one chunk is one of a head chunk corresponding to one end of the data stream, a linking chunk corresponding to an intermediate portion of the data stream, and a tail chunk corresponding to one other end of the data stream.

38. The system of claim 37 wherein the descriptor information includes at least one of head and tail pointers, the head and tail pointers pointing to the head and tail chunks, respectively.

39. The system of claim 38 wherein the connection identifier points to one of the head and tail pointers.

40. The system of claim 34 wherein the controller comprises:

an ingress queue to buffer the data stream of a packet from the ingress of the channel, the packet having a packet size; and

a queue segmenter to chunk the data stream into the at least one chunk.

41. The system of claim 40 wherein the input buffer memory stores the at least one chunk transferred from the queue segmenter.

42. The system of claim 41 wherein the input buffer memory comprises a queue associated with the connection identifier, the queue having a threshold and being configured to store the at least one chunk.

43. The system of claim 34 wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request.

IX. Evidence Appendix

To the best of the knowledge of Appellant, Appellant's legal representative, and Appellant's assignee, there has been no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132, nor has any other evidence been entered in the record by the Examiner and relied upon in this Appeal Brief.

X. Related Proceedings Appendix

To the best of the knowledge of Appellant, Appellant's legal representative, and Appellant's assignee, there are no other appeals or interferences which will directly affect or be directly affected or have a bearing on a decision by the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.